

Haswell-E

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- Intelの新しい高級プロセッサ
- 目玉機能
 - コア部分はHaswellと同じで、速い
 - コア数が最大18コア(E5-2699v3)
 - 4chのDDR4 SDRAM対応 (DDR4-2133)

森藤さんが買った構成

- Core i7 5960X (S-Spec: SR20Q)
 - 8-core, 16-thread, 20M LLC
 - $f_{\max} = 3500\text{MHz}$
- 4x MTA16ATF1G64AZ-2G1A1 1433
 - PC4-2133P-UBZ-10, 8GB
- ASRock X99M Extreme4
 - BIOS P1.30 08/22/2014

DDR4のひみつ

- 真ん中が長い
 - The idea is that when you insert a DDR4 DIMM, it will require less pressure as you'll only be pushing in about half of the pins at a time.

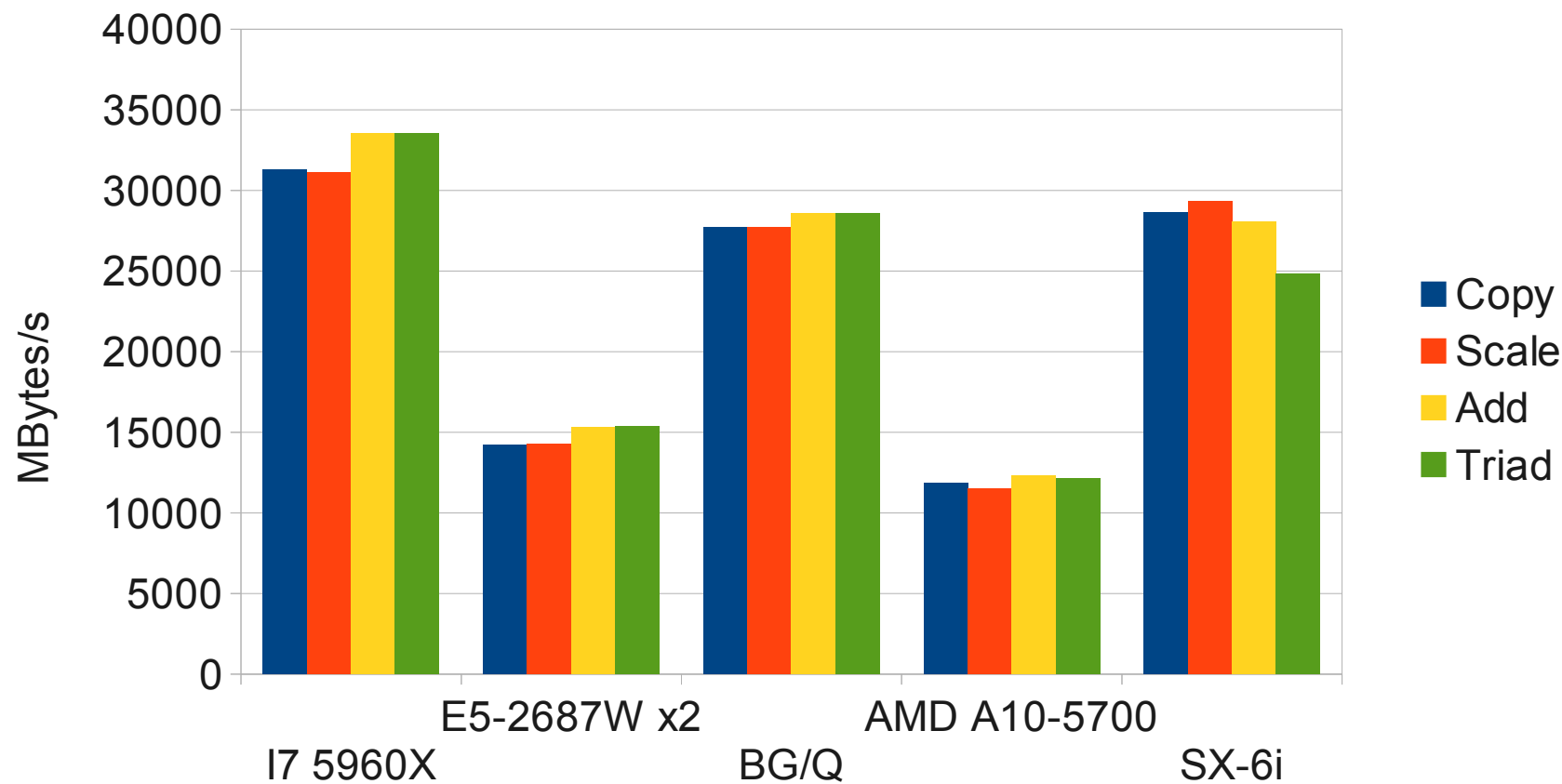


<http://www.anandtech.com/show/6619/>

DDR4の性能

- STREAM (untuned) OpenMP
- 自作読み書きベンチ
 - ベストエフォートtuned

THE STREAMING



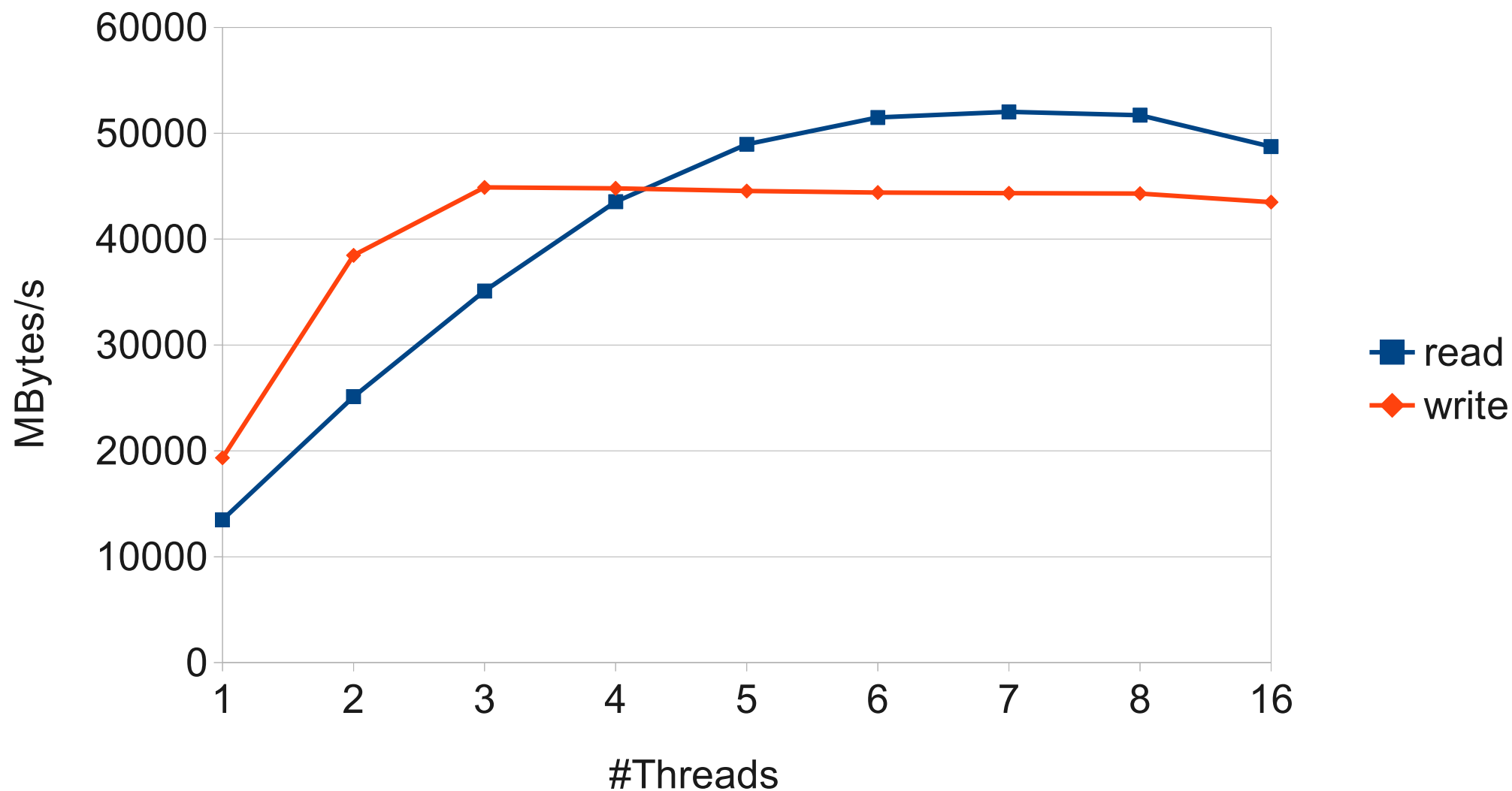
	Type	nCH
I7 5960X	DDR4-2133	4
E5-2687W x2	DDR3-1600	8
BG/Q	DDR3	2
AMD A10-5700	DDR3-1866	2
SX-6i	DDR	

Untuned OpenMP
All available threads

最適化読み書き

- やったこと
 - Prefetch intrinsics
 - Non-temporal store intrinsics
 - Software pipelining

理論値68256MBytes/s ($2133 \times 8 \times 4$)



むすび

- どれくらい先にプリフェッチを飛ばすかを微調整することでもう少しメモリ性能を上げられる
- まだこの機械触って3時間なので粗い部分ある
 - 組み立て・OS導入含む

つらい

- Haswell-EはTSX-NI, HLEが使えない
 - Transactional MemoryとHardware Lock Elision
- 既存プロセッサを含めmicrocode patchで無効化して回っているらしい

HSW136. Software Using Intel® TSX May Result in Unpredictable System Behavior

Problem: Under a complex set of internal timing conditions and system events, software using the Intel TSX (Transactional Synchronization Extensions) instructions may result in unpredictable system behavior.

Implication: This erratum may result in unpredictable system behavior.

Workaround: It is possible for the BIOS to contain a workaround for this erratum.

Status: For the steppings affected, see the *Summary Table of Changes*.