SPARC T4 Fun

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Standpoint of SPARC T4

Historical Aspects of the T4 processor

Brief history of SPARC

- Originally developed by Sun Microsystems (SUNW)
  - Sun originally used Motorola 68000 series in their products: Sun-1, Sun-2, Sun-3.
  - Then they jumped on the RISC bandwagon with Sun-4.

Early SPARC processors

- FPU is integrated on all but the first implementation
- Popular early SPARC processors:
  - TMS390Z50: three-way superscalar
  - RT620: two-way superscalar, higher freq.

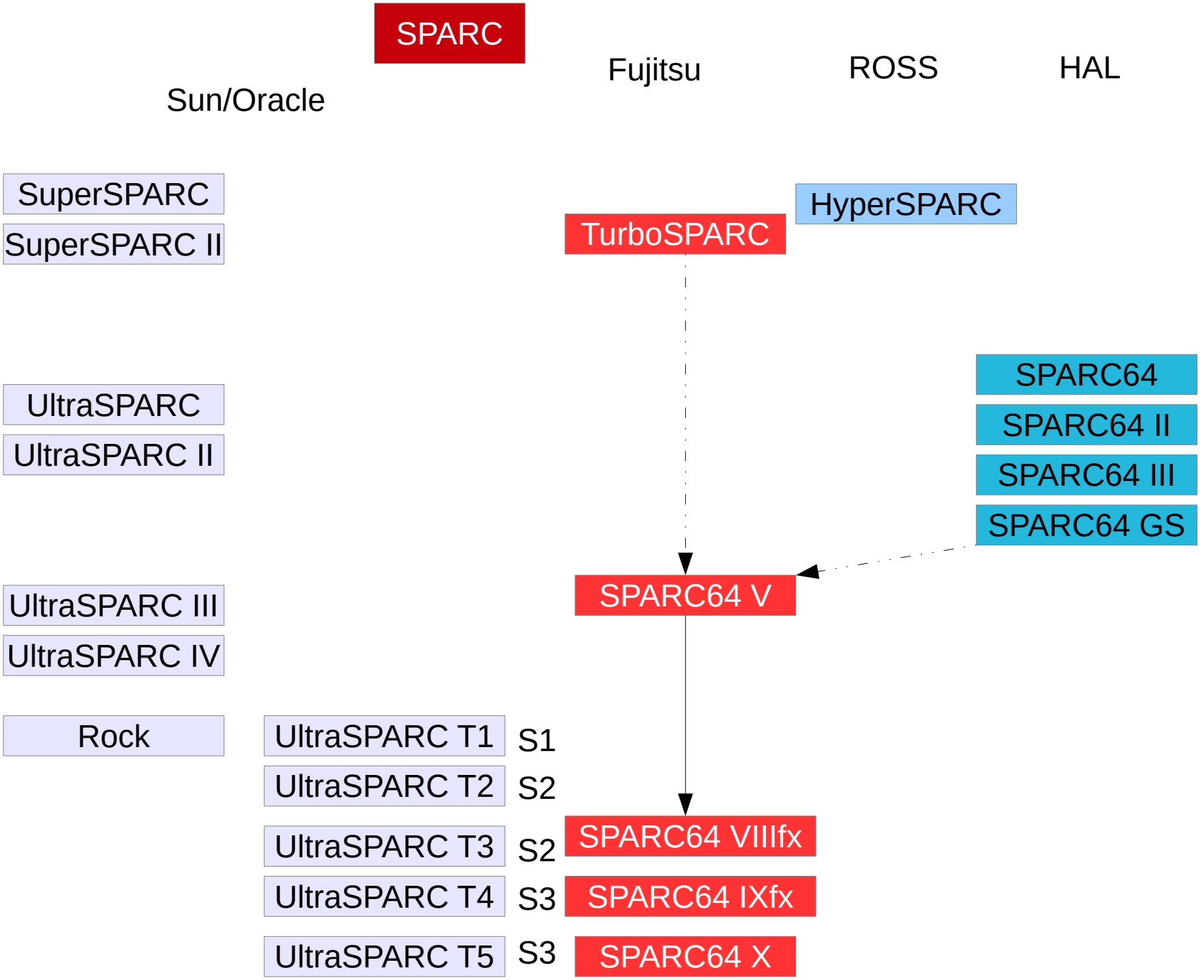
Cypress	602		
Weitek	8601		IPX
Fujitsu	86903		IPX
	86904	microSPARC-II	SPARCstation-5
	86907	TurboSPARC	
TI	TMS390Z50	SuperSPARC	SPARCstation 10
ROSS	RT620	hyperSPARC	

sparcv9

- v9: an extension with 64-bit wide registers and address space
- Implementations:
  - SPARC64 (HAL, later Fujitsu)
  - UltraSPARC (Sun)

Recent SPARC processors

- Sun Rock
  - Transactional memory, Scout threads, Aggressive speculation
  - canceled
- Fujitsu SPARC64 IXfx
  - HPC-ACE: SIMD extension
- UltraSPARC T1, T2, T3, SPARC T4
  - CoolThreads: designed for TLP


SPARC
Sun/Oracle
Fujitsu
ROSS
HAL
SuperSPARC
SuperSPARC II
HyperSPARC
TurboSPARC
SPARC64
SPARC64 II
SPARC64 III
SPARC64 GS
UltraSPARC
UltraSPARC II
UltraSPARC III
UltraSPARC IV
SPARC64 V
Rock
UltraSPARC T1
S1
UltraSPARC T2
S2
UltraSPARC T3
S2
SPARC64 VIIIfx
UltraSPARC T4
S3
SPARC64 IXfx
UltraSPARC T5
S3
SPARC64 X

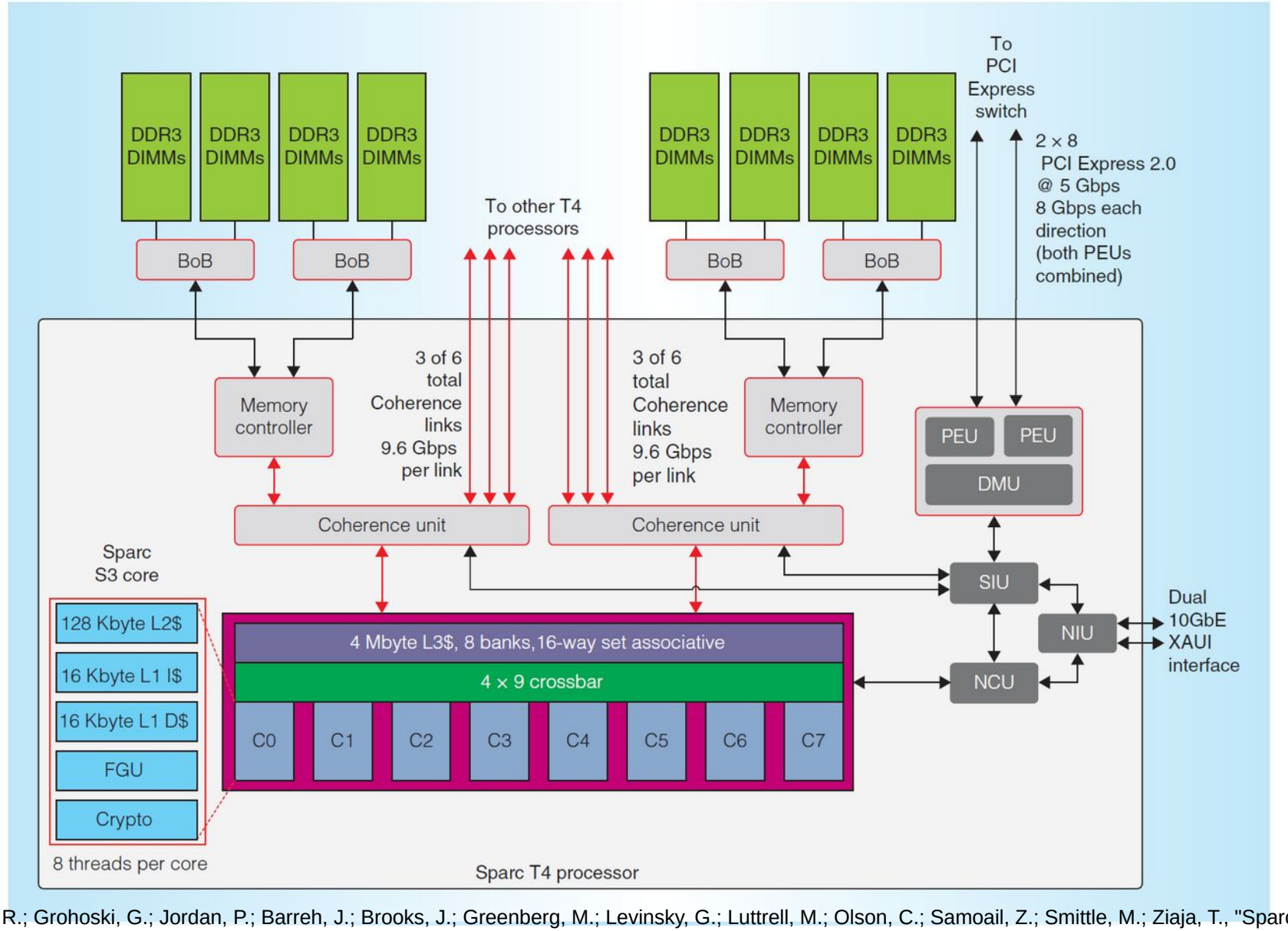
SPARC T4 Architectural Overview

Basic parameters

- 8-core, 8 threads/core => 64 threads/socket
- Processor core is called `S3'
- Manufactured with TSMC 40-nm process
- 855 million transistors, 403 mm2 die size

- Page size 8K, 64K, 4M, 256M, 2Gbytes.
- Page table walking done in hardware (1 walker per chip)

Block diagram



Shah, M.; Golla, R.; Grohoski, G.; Jordan, P.; Barreh, J.; Brooks, J.; Greenberg, M.; Levinsky, G.; Luttrell, M.; Olson, C.; Samoail, Z.; Smittle, M.; Ziaja, T., "Sparc T4: A Dynamically Threaded Server-on-a-Chip," Micro, IEEE , vol.32, no.2, pp.8,19, March-April 2012

Microarchitectural parameters

- Branch prediction: 2-level+Perceptron [Daniel+ 2002]
- New instructions: PAUSE, Compare and Branch, crypt instructions
- 2 instructions/cycle, out-of-order
  - On T3 1 inst/cycle

Cryptographic Acceleration

- Before T4 crypto instructions were privileged
- On T4 they are all user-mode instructions
  - lowers overhead
- AES, CRC, Diffie-Hellman DSA, Elliptic Curve, Kasumi, MD5, RSA, SHA-1
- Multiple-precision multiplications:
  - MPMUL, MONTMUL, MONTSQR
    - 2,048x2,048-bit multiply in 1100 cycles

How to use Solaris on the many-core

System inventory 1/3

- psrinfo -v -p

```
The physical processor has 8 cores and 64 virtual processors (0-63)
  The core has 8 virtual processors (0-7)
  The core has 8 virtual processors (8-15)
  The core has 8 virtual processors (16-23)
  The core has 8 virtual processors (24-31)
  The core has 8 virtual processors (32-39)
  The core has 8 virtual processors (40-47)
  The core has 8 virtual processors (48-55)
  The core has 8 virtual processors (56-63)
    SPARC-T4 (chipid 0, clock 2848 MHz)
The physical processor has 8 cores and 64 virtual processors (64-127)
  The core has 8 virtual processors (64-71)
  The core has 8 virtual processors (72-79)
  The core has 8 virtual processors (80-87)
  The core has 8 virtual processors (88-95)
  The core has 8 virtual processors (96-103)
  The core has 8 virtual processors (104-111)
  The core has 8 virtual processors (112-119)
  The core has 8 virtual processors (120-127)
    SPARC-T4 (chipid 1, clock 2848 MHz)
```

System Inventory 2/3

- prtdiag -v

  sun4u - UltraSPARC, ... ,UltraSPARC IV

  sun4v - T1, ... : supports virtualization (LDOM)

System Configuration: Oracle Corporation sun4v SPARC T4-2
Memory size: 65024 Megabytes

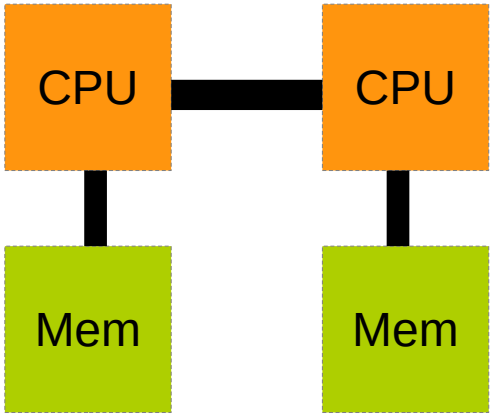
========== Virtual CPUs ==========

CPU ID	Frequency	Implementation	Status
0	2848 MHz	SPARC-T4	on-line
1	2848 MHz	SPARC-T4	on-line

System Inventory 3/3

- lgrpinfo

  locality group




```
lgroup 0 (root):
        Children: 1 2
        CPUs: 0-127
        Memory: installed 64G, allocated 16G, free 48G
        Lgroup resources: 1 2 (CPU); 1 2 (memory)
        Latency: 18
lgroup 1 (leaf):
        Children: none, Parent: 0
        CPUs: 0-63
        Memory: installed 32G, allocated 4.8G, free
27G
        Lgroup resources: 1 (CPU); 1 (memory)
        Load: 0.0155
        Latency: 12
lgroup 2 (leaf):
        Children: none, Parent: 0
        CPUs: 64-127
        Memory: installed 32G, allocated 11G, free 21G
        Lgroup resources: 2 (CPU); 2 (memory)
        Load:    0
        Latency: 12
```

Solaris for Linux users

- tar (sysv tar) vs. gtar (GNU tar)
  - GNU tar supports gnu extensions
  - GNU tar required for extracting OSS tarballs
- make (sysv make) vs. gmake (GNU make)
  - Makefile syntax is different
- m4 (sysv m4)
- sed, awk

Development Infrastructure

- Compiler: Solaris Studio 12.3
  - Installed in /opt/solarisstudio12.3
  - Beginning with v12.3, no symlink is installed in /usr/bin by default
    - set your PATH env. var.
- as, ld is in /usr/ccs/bin
  - GNU Binutils on SunOS/SPARC has been broken for years

Compiling GCC on Solaris

- export ABI=32 and compile GMP, MPFR, MPC
- My favorite compiling option is:

  ../gcc-4.5.4/configure --prefix=/home/tomari/gcc45 --with-gmp=/home/tomari/gcc45 --with-mpfr=/home/tomari/gcc45 --with-mpc=/home/tomari/gcc45 --disable-nls --enable-languages=c,c++,fortran --disable-libssp --with-system-zlib --with-as=/usr/ccs/bin/as --with-ld=/usr/ccs/bin/ld

Controlling Process

- Set affinity to locality group
  - plgrp
    - env OMP_NUM_THREADS=64 plgrp -A 1/strong -e ./bt.A.x
  - This binds bt.A.x to a socket
- Bind process to processor(s)
  - pbind (after creating the process, e.g. shell)
  - psrset

How to use psrset

- psrset -c 0-7 (create processor set)
- psrset -c 8-15
- psrset -c 64-71
- psrset -i (display sets)
- env OMP_NU..=8 psrset -e 1 ./cg.A.x
- A processor can be assigned to a single processor set; when assigned, a processor runs only LWP assigned to the processor set

Modify privileges for psrset and dtrace

- psrset can be dangerous for a time-sharing system, privilege required for operation.
- usermod -K defaultpriv=basic,sys_res_config,dtrace_kernel,dtrace_proc,dtrace_user tomari
  - This enables use of dtrace and psrset for user tomari

Solaris Processor Fun

- psradm
  - Disable interrupt handling on specified processor
    - psradm -i 1 2
  - Turns processors 1 and 2 to no-intr mode
  - may reduce OS jitter on the processors 1 and 2
- Same config can be created with psrset too:
  - psrset -f 1
- Check status with psrinfo -v

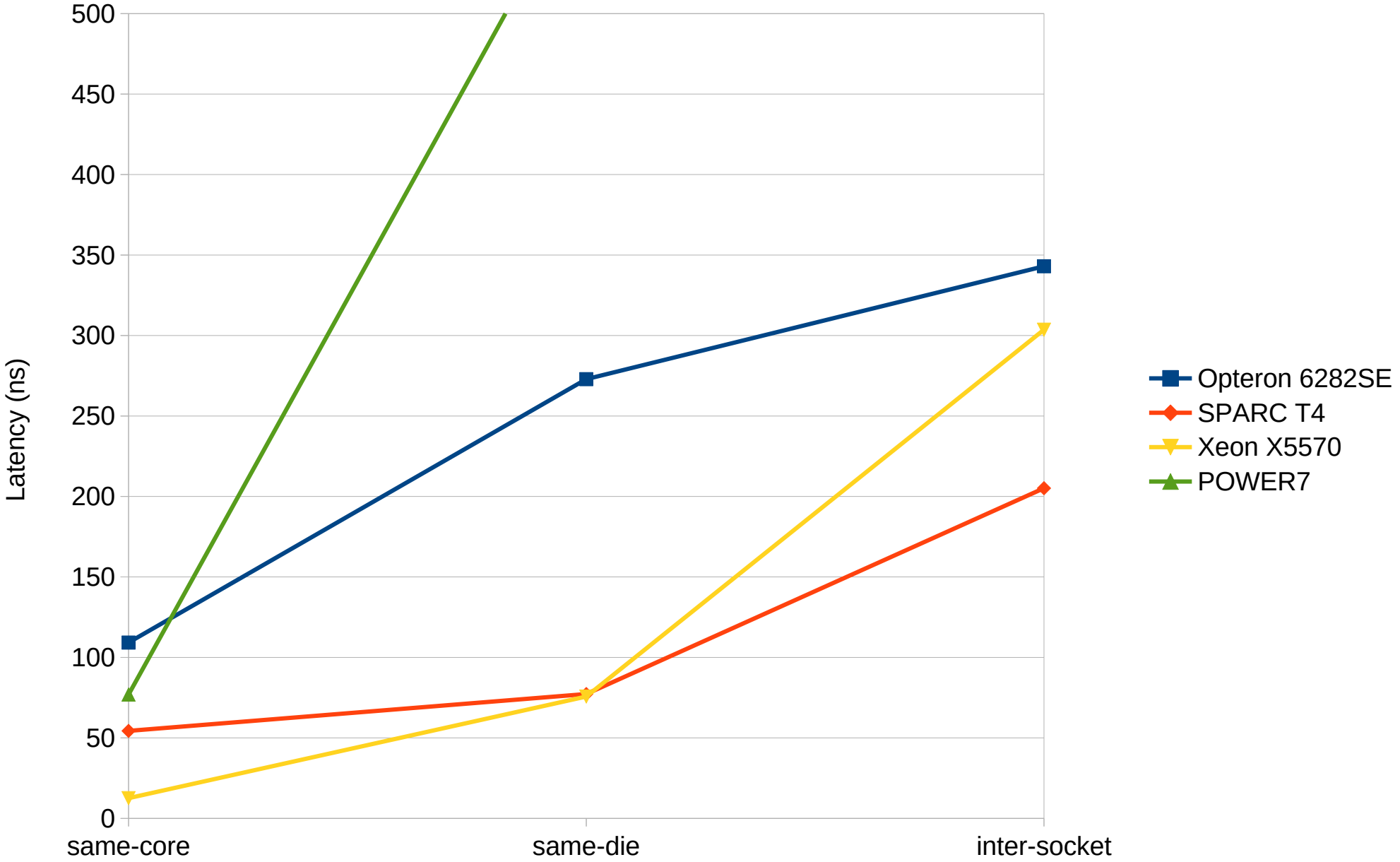
```
Status of virtual processor 0 as of: 03/10/2013
19:53:59
  no-intr since 03/10/2013 19:53:35.
  The sparcv9 processor operates at 2848 MHz,
        and has a sparcv9 floating point processor.
```

Benchmark results

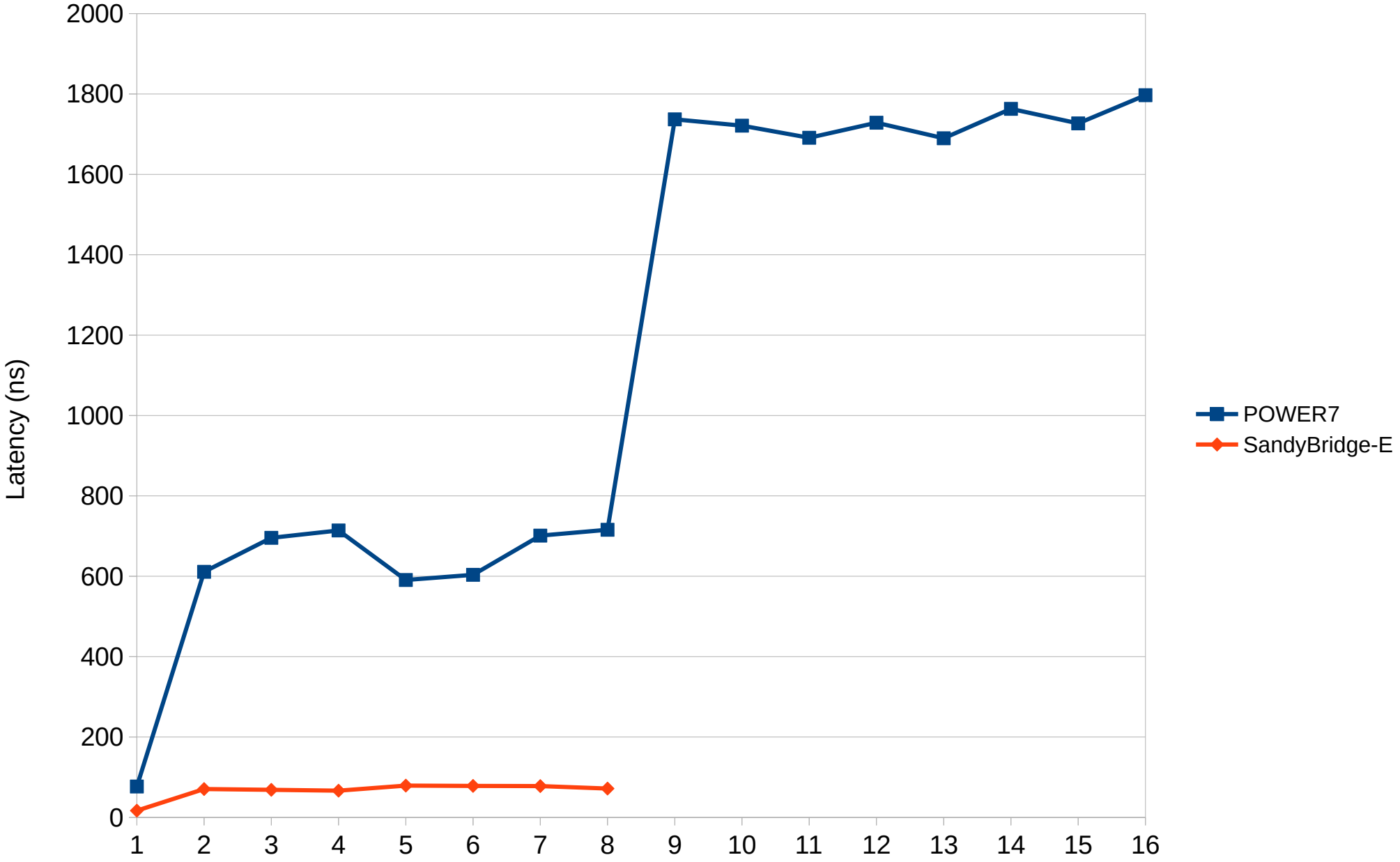
Inter-thread latency

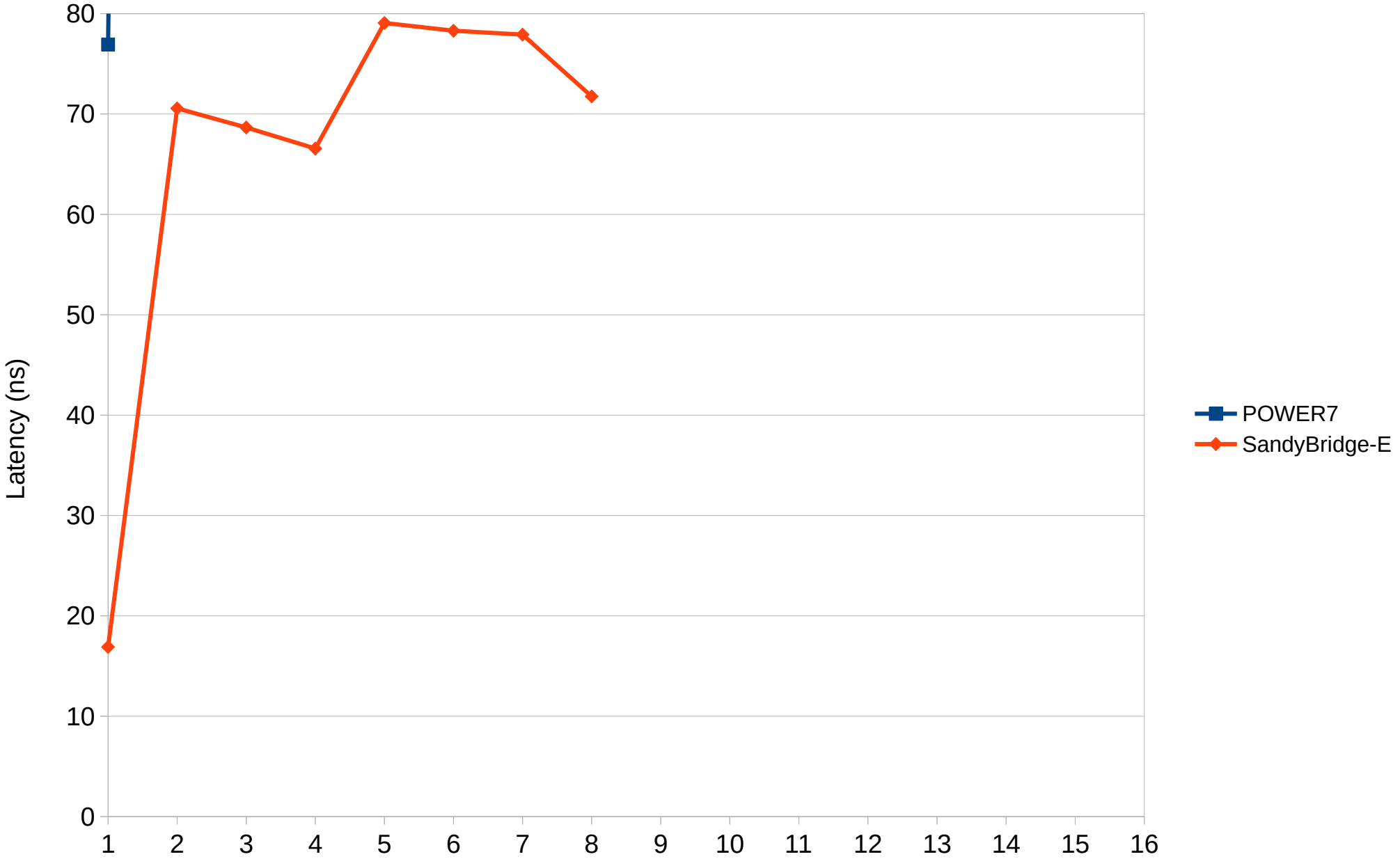
- Measure ping-pong latency between threads
- Repeat Compare-and-Swap
- Bind thread to same/different physical core or socket
  - use psrset command
- The benchmark is on
  - https://github.com/tomari/shmlatency

Latency results

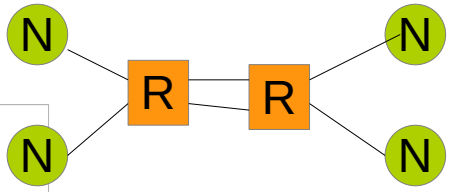


Latency with Nonuniform NoC



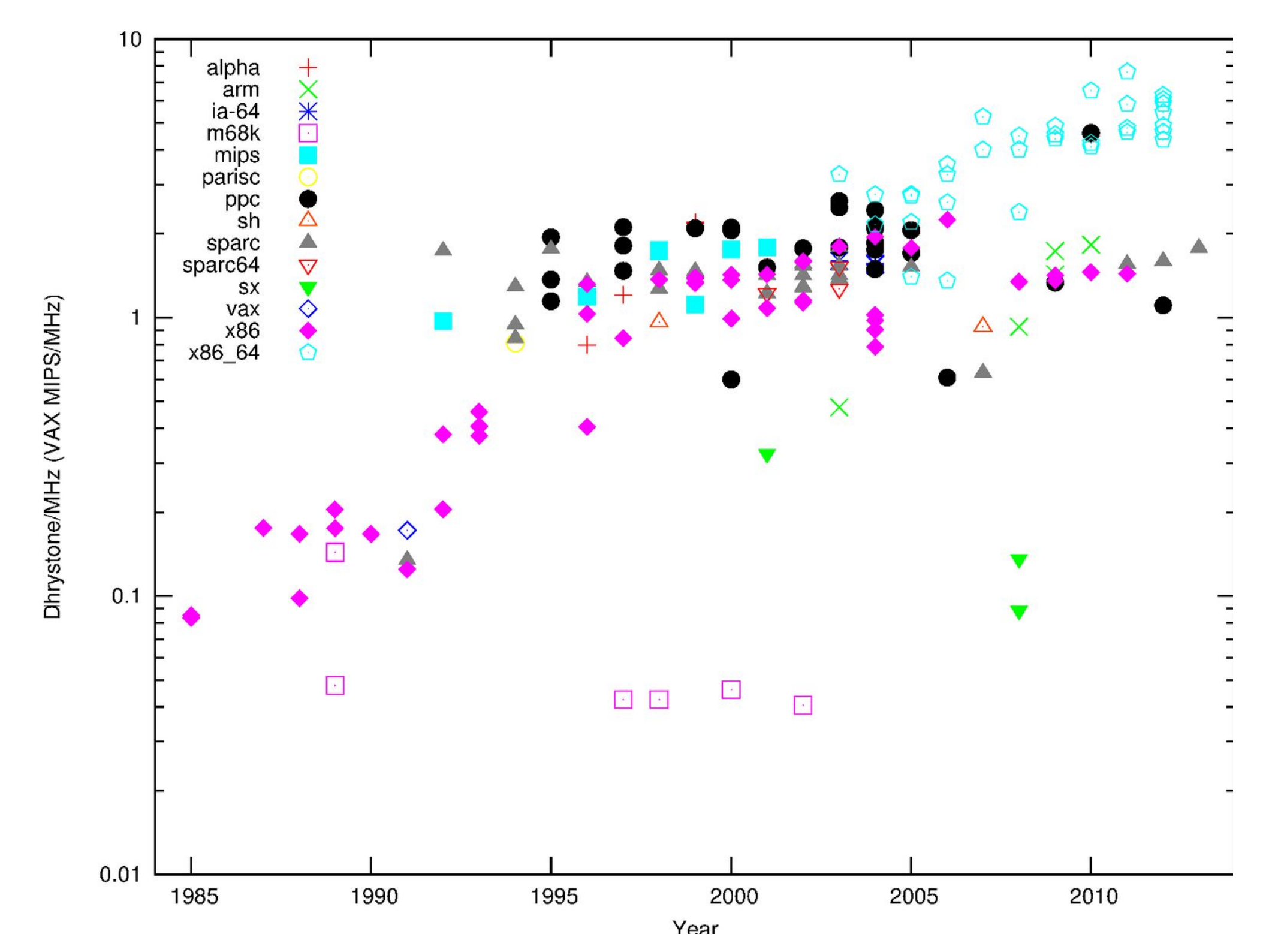

Latency (ns)
0
10
20
30
40
50
60
70
80
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
POWER7
SandyBridge-E

Power7 vs Historic Parallel Machines

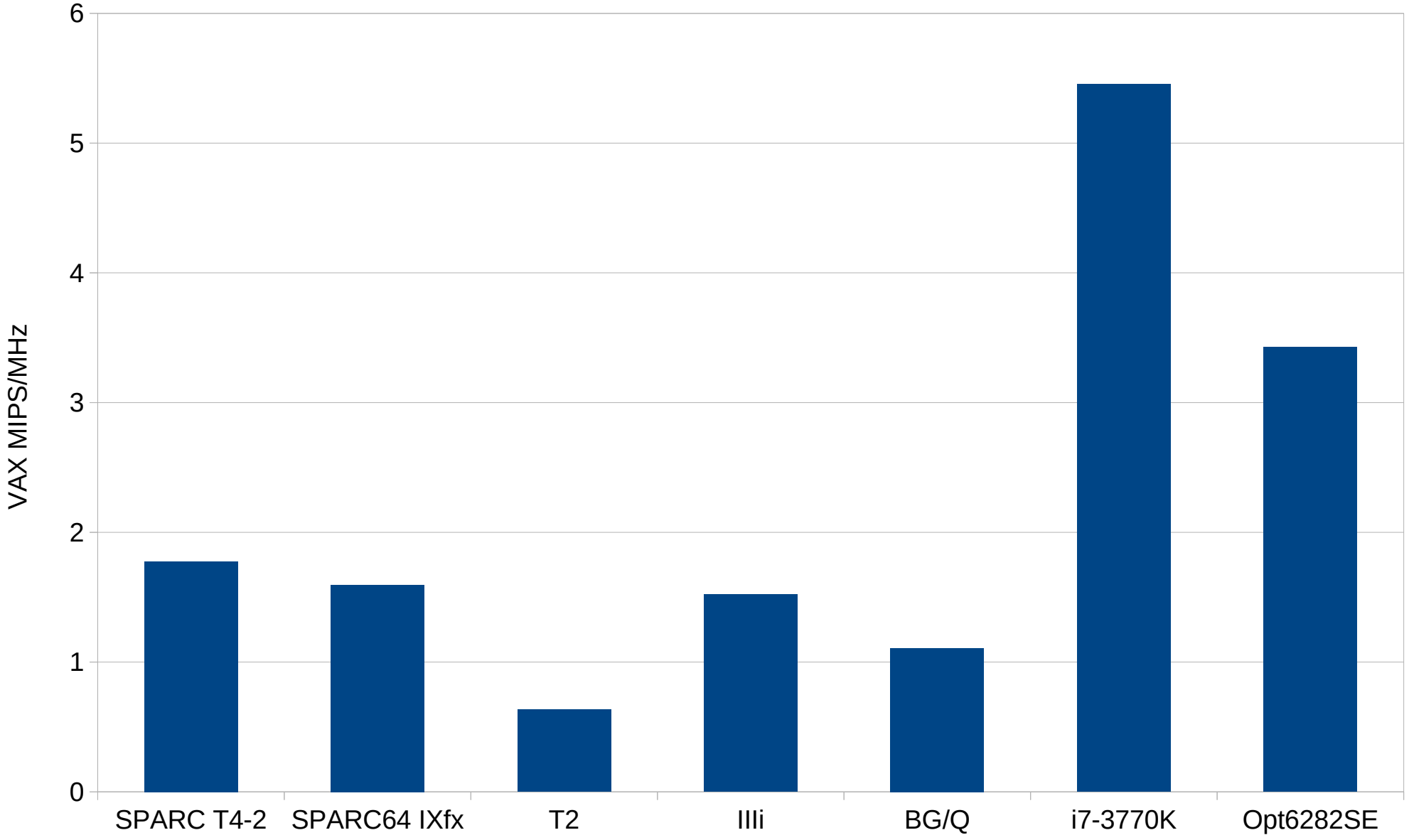


Single-thread Performance

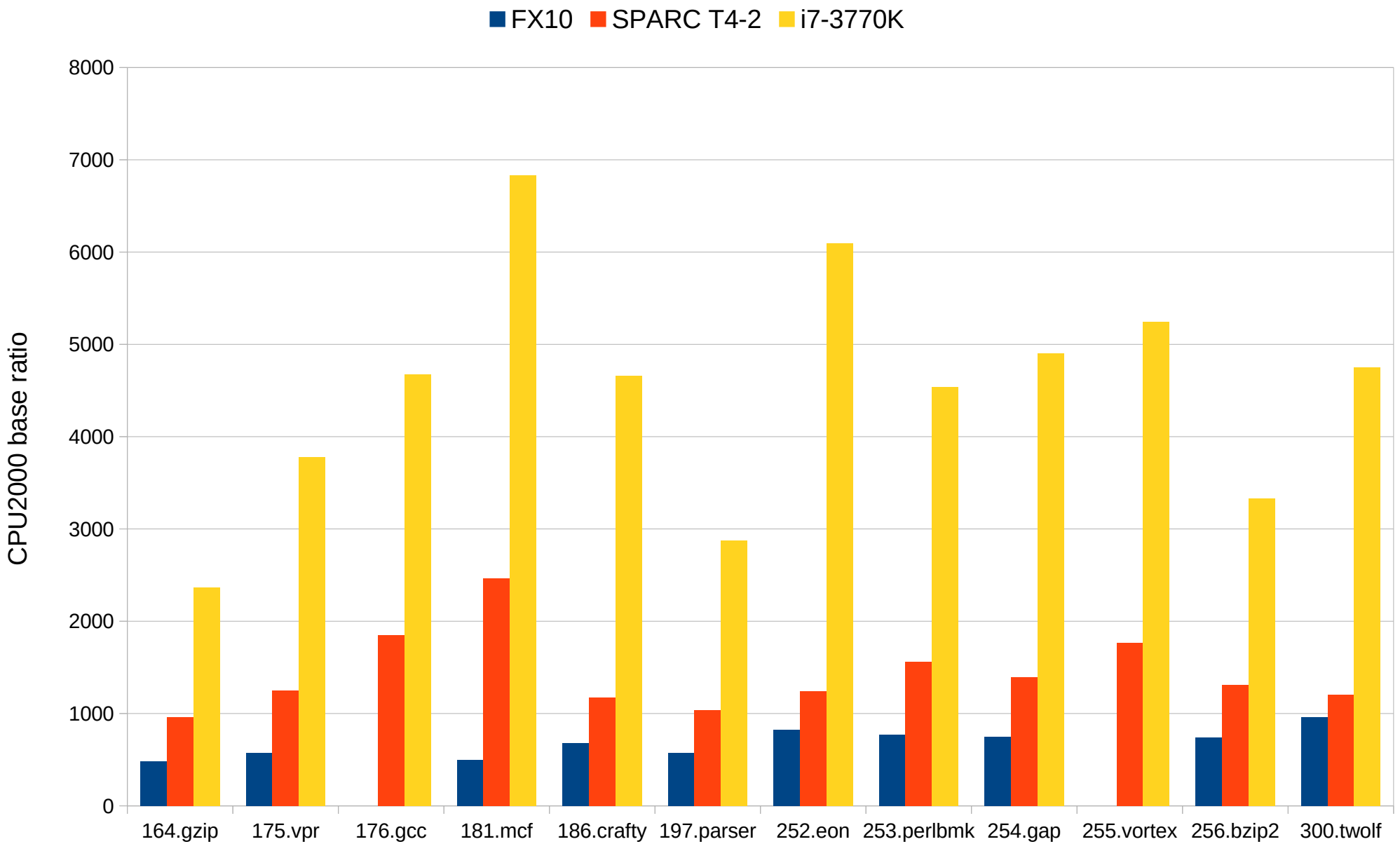
- Dhrystone
  - Small, yet results are close to SPEC CPU200x.
  - Compare both old and new systems
- SPEC CPU2000
  - Standard benchmark suite for architectural study


alpha
arm
ia-64
m68k
mips
parisc
ppc
sh
sparc
sparc64
sx
vax
x86
x86_64
Dhrystone/MHz (VAX MIPS/MHz)
10
1
0.1
0.01
1985
1990
1995
2000
2005
2010
Year

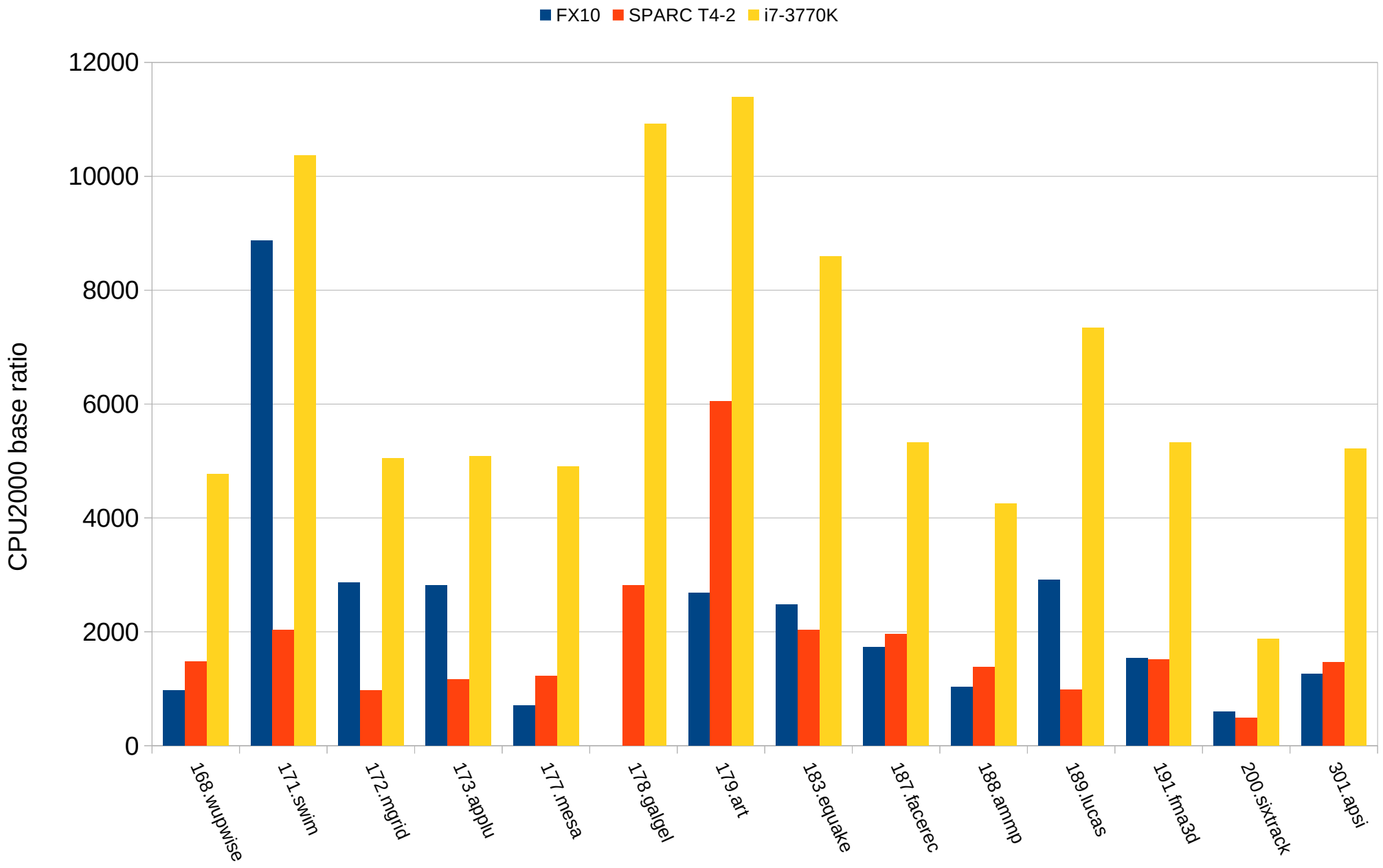
Dhrystone/MHz



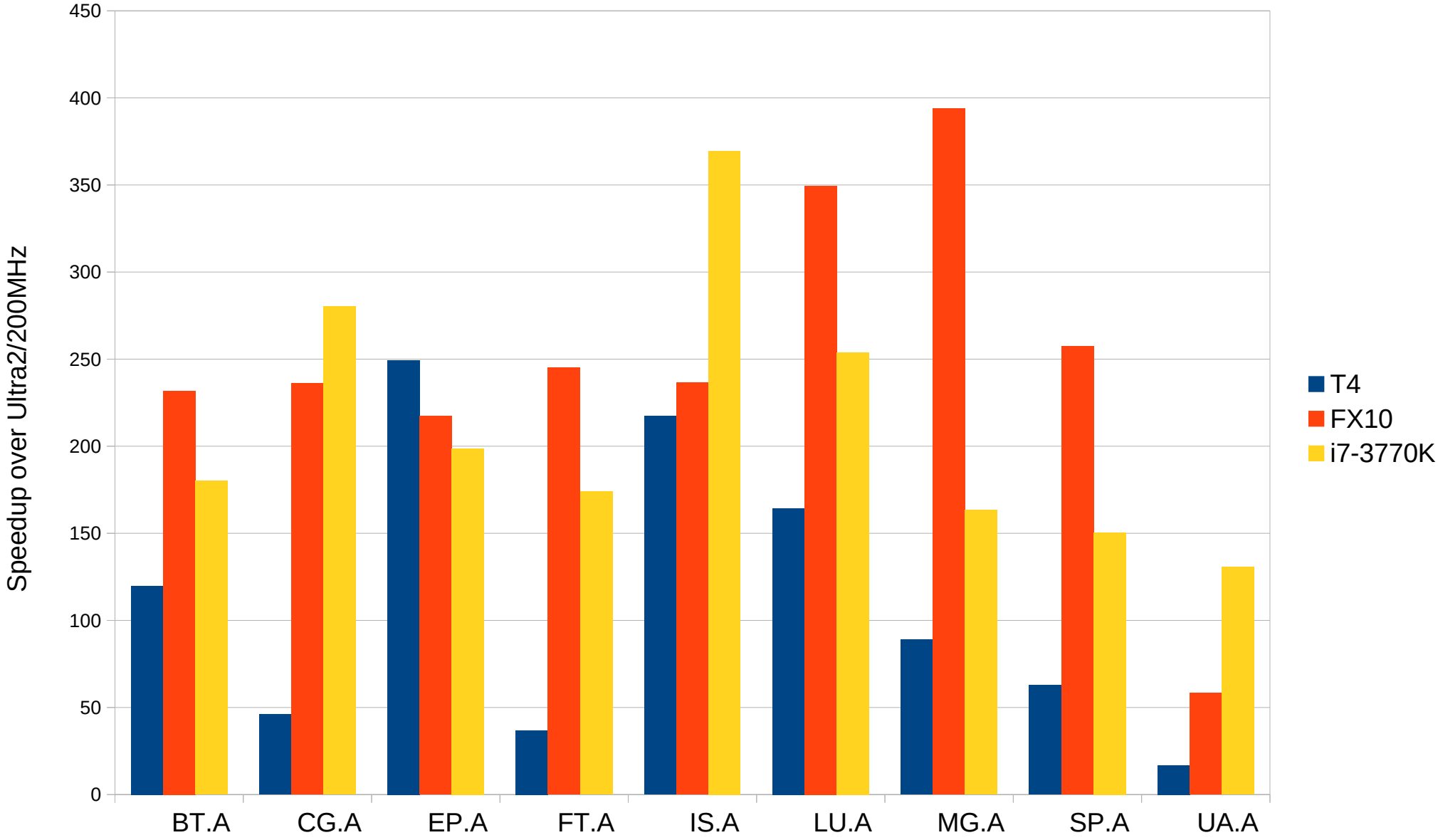
CINT2000


FX10
SPARC T4-2
i7-3770K
CPU2000 base ratio
8000
7000
6000
5000
4000
3000
2000
1000
0
164.gzip
175.vpr
176.gcc
181.mcf
186.crafty
197.parser
252.eon
253.perlbmk
254.gap
255.vortex
256.bzip2
300.twolf

CFP2000


FX10
SPARC T4-2
i7-3770K
CPU2000 base ratio
12000
10000
8000
6000
4000
2000
0
168.wupwise
171.swim
172.mgrid
173.applu
177.mesa
178.galgel
179.art
183.equake
187.facerec
188.ammp
189.lucas
191.fma3d
200.sixtrack
301.apsi

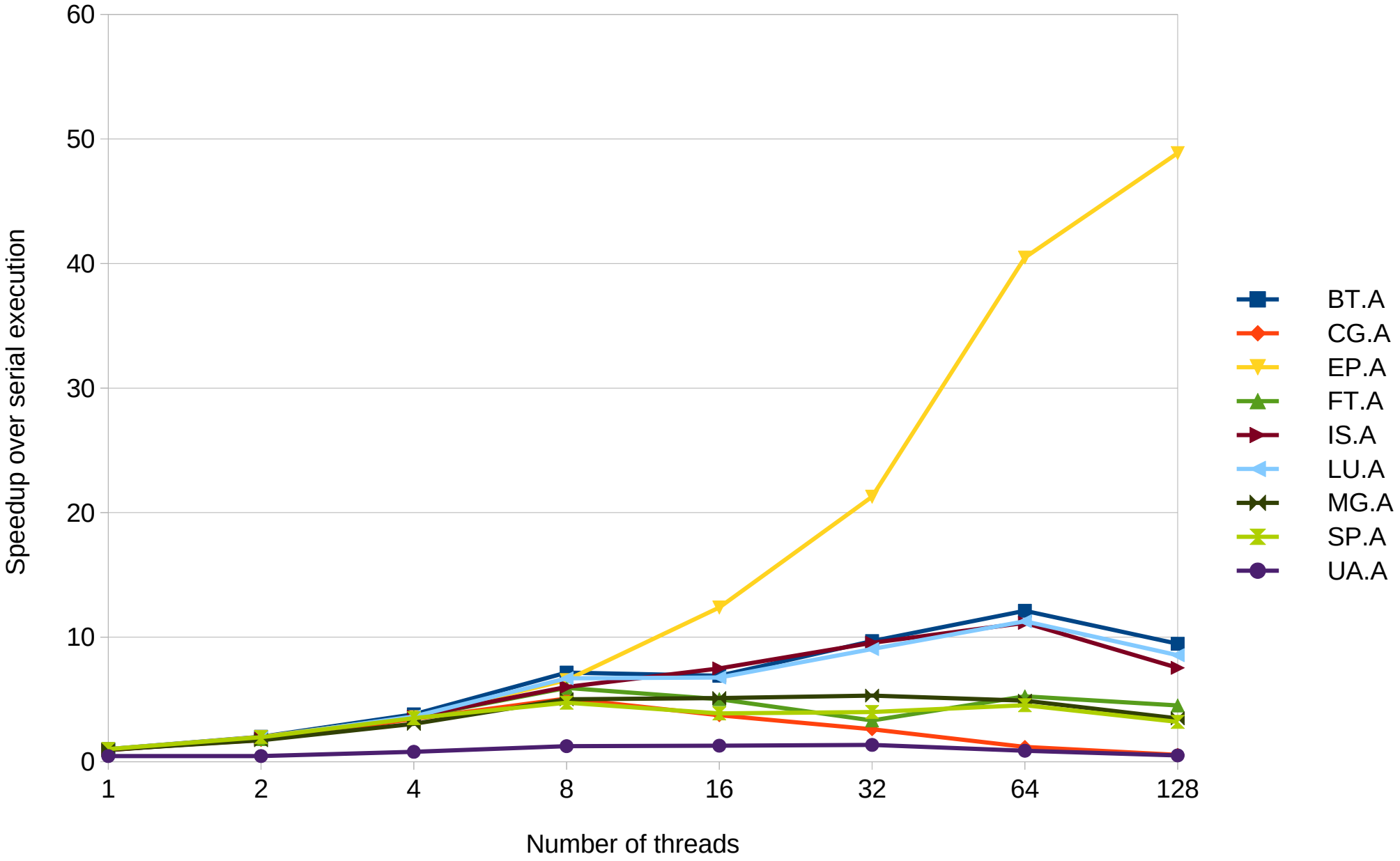
NPB-OMP/socket



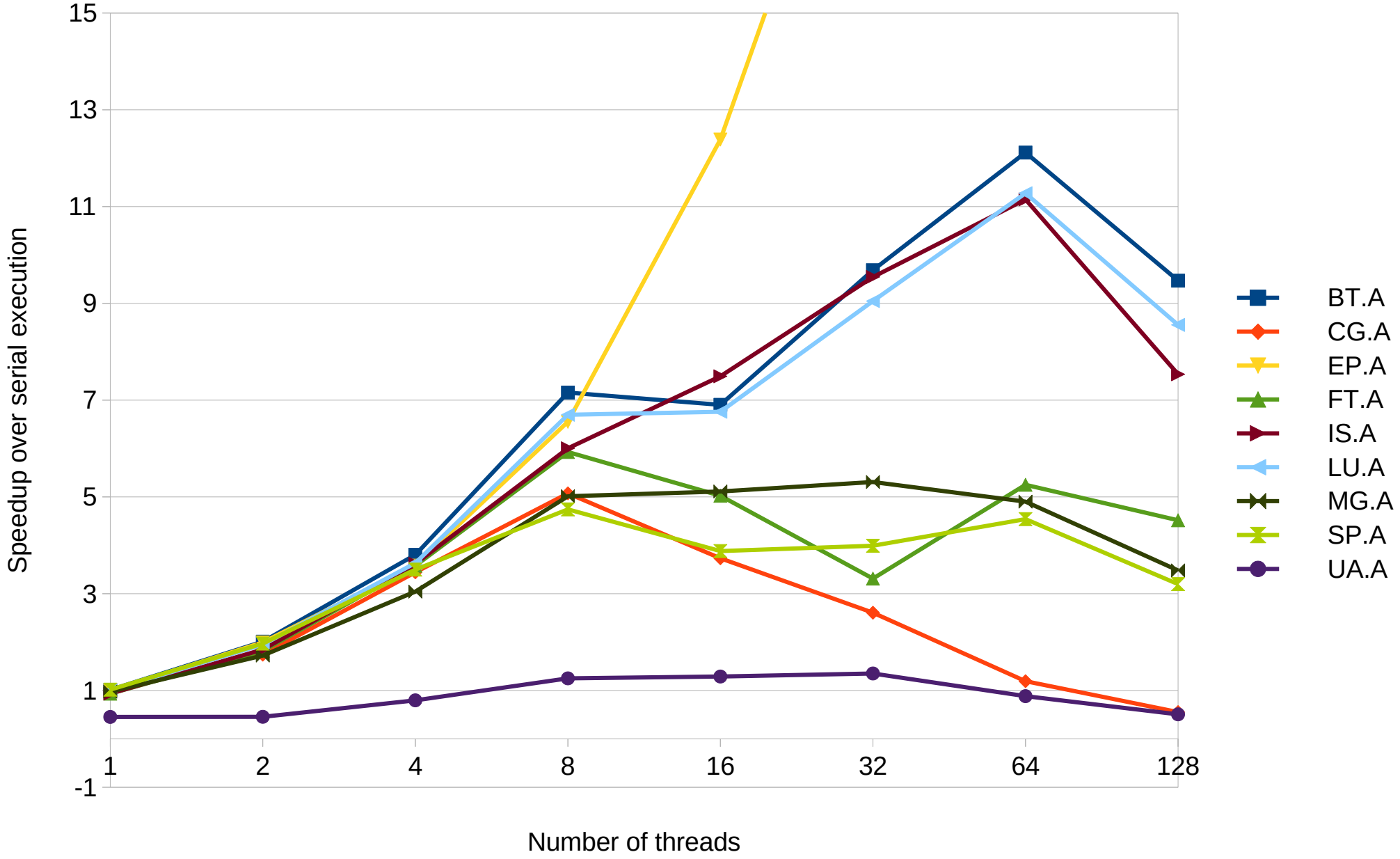
NPB OpenMP Scalability

- Run NPB with varying number of threads
- Optimal thread count per physical core?

NPB OMP Speedup



NPB OMP Speedup



Conclusion

- SPARC T4 architecture was reviewed
- Solaris incorporates advanced features necessary for large-scale, many-core computing
  - Usage is described
- Performance characteristics was observed with well-proven and mini benchmarks